

1 **ABSTRACT OF THE DISCLOSURE**

2 The invention encompasses stacked semiconductor devices including
3 gate stacks, wordlines, PROMs, conductive interconnecting lines, and
4 methods for forming such structures. In one aspect, the invention
5 includes a method of forming a conductive line comprising: a) forming
6 a polysilicon layer; forming a silicide layer against the polysilicon layer;
7 b) providing a conductivity-enhancing impurity within the silicide layer;
8 and c) providing the polysilicon layer and the silicide layer into a
9 conductive line shape. In another aspect, the invention includes a
10 programmable-read-only-memory device comprising: a) a first dielectric
11 layer over a substrate; b) a floating gate over the first dielectric layer;
12 c) a second dielectric layer over the floating gate; d) a conductive line
13 over the second dielectric layer; and e) a metal-silicide layer over the
14 conductive line, the metal-silicide layer comprising a Group III dopant
15 or a Group V dopant.

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